NON-BLOCKING, MULTI-CONTEXT PIPELINED PROCESSOR

ABSTRACT OF THE DISCLOSURE

A packet processor whose processing capabilities are optimized by concurrently processing multiple packets within various pipelined stages. At each stage, multiple packets are processed via an internally pipelined sub-processor. In one embodiment, the packets are processed in a round robin fashion. When a particular packet is done processing at a particular stage, it may pass another packet whose processing is not complete, and move to a next stage. In another embodiment, a packet is processed until a conditional branch instruction or any other instruction causing a potential stall is encountered. If such an instruction is encountered, a next available packet is selected and processed instead of wasting processing cycles during the stall, or proceeding with the processing of the current packet based on a predicted result. The sub-processor resumes processing of the packet once the stall is over.